ENEE245: Digital Circuits and Systems Laboratory (Spring 2019)

1. General Information

Time: Lecture 31307 T/R 1:00PM - 1:25PM Location: SC416
Lab 31308 T/R 1:30PM – 2:45PM Location: SC416

Instructor: Professor Lan Xiang (Science Center 436F)
Email: Lan.Xiang@montgomerycollege.edu
Phone: (240) 567-1740
Office Hours: MW 12 – 1:00pm, 2:30pm – 3:00pm, TR 9:00am – 10:00am

Course Webpage: http://cms.montgomerycollege.edu/lxiang

Required Texts and Materials:

1. *Starter's Guide to Verilog 2001*, ISBN 9780131455560, Prentice Hall, by Michael D. Ciletti.
2. ENEE244 textbook: *Introduction to Logic and Computer Design*, 1st Edition, McGraw-Hill, by A. Marcovitz; or *Digital Design*, 5th Edition, Prentice Hall, by Morris Mano.
3. Each student is required to purchase a Breadboard and a Jumper Wire Kit (available at MC Bookstore). The kit is also used in ENEE207.
4. Each student will receive a package containing all the components in the beginning of the semester. Before the last day of the class, the component package must be returned to the lab staff at SC419 promptly in order to receive the full credit of the last lab report grade.

2. Course Objective:

Introduction to basic measurement techniques and electrical laboratory equipment such as design, construction, and characterization of digital circuits containing logic gates, sequential elements, oscillators, and digital integrated circuits; introduction to digital design and simulation with the Verilog Hardware Description Language (HDL).

PREREQUISITES: *PHYS262, ENEE244, and a grade of C or better in ENEE150 or CMSC204. One hour lecture, three hour laboratory each week.*

3. Course Outcomes:

Upon completion of this course a student will be able to

a) Use simulation, test, and measurement equipment necessary to evaluate the functionality and performance of simple circuits
b) Demonstrate an understanding of basic limitations, inaccuracies, and tolerances of the test equipment, components, and procedures
c) Design digital circuits and systems to efficiently, reliably, and economically achieve desired results
d) Master techniques for modeling circuits and systems through structural and gate-level networks, and breadboarding designs; trouble shooting circuits and systems
e) Use hardware description languages and simulation tools to design circuits and systems and analyze their performance
f) Document experiments using an industry recognized report format

4. Grading Policy:

Prelabs	10%
Homework	10%
In Lab Performance	20 %
Lab Reports	40 %
Final Exam	20 %
Total	100 %

The final grade is based on the following:

A	90 – 100%
B	80 – 89%
C	70 – 79%
D	60 – 69%
F	below 60%

NOTES:

1. Late Policy: If a student has any documented excused lateness or absence, please talk to the instructor within 24 hours for special arrangement. **Make-up exams** will be allowed **ONLY** for documented excused absences and with prior permission from the instructor. No late submission of prelab and homework will be accepted. Each student is required to write a formal lab report (check the lab guideline and lab report rubrics on the course website) unless it is specified otherwise. For lab reports, students are permitted up to **THREE TIMES ONE-DAY** lateness (email by Wednesday midnight) without penalty. No other late turn in of reports will be accepted for any reason.

2. **Attendance**: Each student is required to attend the class on time every time. Late for more than 15 minutes will be marked as an absence. Two or more unexcused absences without prior permission from the instructor will receive 10% penalty towards the final grade.

3. **Support Services**: Any student who may need an accommodation due to a disability, please make an appointment to see me during my office hour. A letter from Disability Support Services authorizing your accommodations will be needed. Any student who may need assistance in the event of an emergency evacuation must identify to the Disability Support Services Office; guidelines for emergency evacuations for individuals with disabilities are found at *http://www.montgomerycollege.edu/dss/evacprocedures.htm*.

4. **Academic Honesty**: All homework, quizzes, labs, and examinations are to be the results of a student's own efforts. Any cheating, copying, or academic dishonesty could result in a failing grade for the assignment and the course. You may not copy from one another. You may also not give any paper or electronic copies of any parts of your homework or lab reports to other students to look at.

In addition to course requirements and objectives that are in this syllabus, Montgomery College has information on its web site (see link below) to assist you in having a successful experience both inside and outside of the classroom. It is important that you read and understand this information. The link below provides information and other resources to areas that pertain to Student Success such as: Student Behavior (Student Code of Conduct); Student e-mail, College Tobacco Free Policy; Course Withdrawal and Refund Information; Resources for Military Service Members, Veterans and Dependents; how to access information on delayed openings and closings; how to register for Montgomery College's Alert System and how closings and delays can impact your classes.
Important Student Information Link: http://cms.montgomerycollege.edu/mcsyllabus/

ENEE 245 Course Outline (Spring 2019)

Wk	DATES	TOPICS	NOTES
1	1/22, 1/24	Introduction to the Course Lab 0: Introduction to Test and Measurement Equipment	Lab report 0 due 1/29
2	1/29, 1/31	Lab 1: Simple Combinational Logic Circuit (No simulation is required.)	Lab report 1 due 2/5
3	2/5, 2/7	Lab 2: Introduction to Quartus II CAD and Verilog HDL - Schematic Design Entry - Verilog Design Entry - Functional and Timing Simulations	Lab report 2 due 2/12
4	2/12, 2/14	Lab 3: Introduction to FPGA Development Board - Altera DE2-115 Board - FPGA Implementation and Testing (Pin Assignments)	No lab report.
5	2/19, 2/21	Lab 4: Adder Circuits: Full Adder, Ripple Carry Adder, and Carry Look-ahead Adder - 1-bit Full Adder - Rise and Fall time, Delay time - 4-bit Ripple Carry and Carry Look-ahead Adders - Seven Segment Display	Lab report 4 due 3/5
6	2/26, 2/28	Continue Lab 4	
7	3/5, 3/7	Lab 5: Decoders and Encoders - 3 to 8 decoder - 8 to 3 encoder and priority encoder	Lab report 5 due 3/19
8	3/12, 3/14	**SPRING BREAK**	
9	3/19, 3/21	Lab 6: Binary Counters - Synchronous Counters (structural and behavioral) - Synchronous vs. asynchronous clear - Generate 1Hz clock	Lab report 6 due 3/26
10	3/26, 3/28	Lab 7: Encryption Sequence Detector - Shift registers and JK Flip-Flops - Finite State Machine	Lab report 7 due 4/9
11	4/2, 4/4	Continue Lab 7	
12	4/9, 4/11	Lab 8: Multiplier Circuits	Lab report 8 due 4/23
13	4/16, 4/18	Continue Lab 8	
14	4/23, 4/25	Lab 9: A Digital Calculator -Addition, Subtraction, Multiplication & Division	Lab report 9 due 5/2
15	4/30, 5/2	Finish Lab 9. Final Review	
16	**Final Exam: May 9, 2019 Thursday, 12:30PM– 2:30PM, SC416**		

ENEE245 Lab Guideline

Guidelines for Lab Report:

Writing useful reports is a very essential part of becoming an engineer. In both academic and industrial environments, reports are the primary means of communication between engineers. In general, the lab reports for this class should follow the following guidelines and format:

1. Reports should completely document the laboratory activity so that the reader can reconstruct the work completed without any knowledge of the laboratory handout. **Do not copy the requirements or procedures from the laboratory handout.** Instead, you should write down what you have done in the lab in your words. The report should include sufficient detail in order for the reader to adequately follow the steps. Be clear and concise.
2. **Typed Reports are required.** Free hand writings and drawings will not be accepted unless specified by the instructor.
3. **Label and annotate all included tables, drawings, and attached figures.** Graphs and tables should be clear and logical. They should be free-standing and carefully labeled, so that the reader can understand them without referring to the text. Hence, you will have to choose figure captions and table titles carefully. For example, you got a printout of the voltage across resistor R1 from your digital oscilloscope and you included that printout in your report. You may label and annotate the printout as Figure 1: voltage across resistor R1. Then in your report, when you describe the procedures you have done in the lab, you may explain that you displayed and measured the voltage across the resistor R1 using digital oscilloscope, the printout is shown in Figure 1.
4. **Explain your results along with necessary discussions.** Attach necessary figures to show how you get the results. Printouts are not your final results. You need to explain and comment on the results and make a conclusion whether you have met the requirements or not.
5. **Documentation of your source codes.** All your source codes of the Verilog design files should be well documented.
6. **Each student must submit an individual report based on an individual effort.** Results should not be shared among the students. You may not give any paper or electronic copies of any parts of your work to other students to look at. Academic dishonesty will not be tolerated.
7. **Check with each lab report rubrics.** Each lab report rubrics is on the course website.

Lab Report General Format:

TITLE PAGE: The title page or a title block should always include the lab experiment number and the title, the date it was submitted or due, and your name.

OBJECTIVE: The objective of your experiment should be brief and clear. It should state the objectives of the experiment, but in your words. Do not simply "copy" the objectives from the lab manual.

DESIGN: This section should include the theory related to the design of the circuit schematic or Verilog code. Use diagrams, tables or Boolean functions to illustrate your design. Discuss the design specifications, show circuit/Verilog implementation and what each portion of the circuit/Verilog code was representing. Circuit schematics should be also included in this section. Your graded prelab cannot be used as the design.

HARDWARE: This section should include any equipment or materials used in the lab experiment.

EXPERIMENT: This section describes the experimental process (both simulation and circuit) and corresponding results in the order they actually happened. Using subsections and a clear paragraph structure as needed. DO NOT COPY AND PASTE DIRECTLY FROM THE LAB MANUAL. Where appropriate, you should describe what you did in each step and show your results, with a schematic, graph, data, calculations, or perhaps a brief statement. Attach figures if needed. But be sure to label and refer to all the figures and tables. All the results and calculations should be included with **clear explanations**.

ANALYSIS: This is a very important part of your report. You should show, in this section, that you understand the experiment beyond the simple level of completing it. You should analyze your results of the experiment; compare expected results with those obtained; analyze experimental errors; relate results to your experimental objectives and what you have learned from ENEE244; and respond to all questions outlined in the experiment if any. You may include the discussions about any difficulty or unexpected results about the experiment and how they were solved (or why they were ignored).

CONCLUSIONS: This section should present overall conclusions relating to the original purpose of the experiment. Comment on the outcome of what you did. Typically, the conclusion section of a lab report demonstrates what was learned from the experiment.